32/5/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04268922 E.I. No: EIP95102892915
Title: Exploring configurations of functional units in an out-of-order superscalar processor
Author: **Jourdan, Stephan** ; Sainrat, Pascal; Litaize, Daniel
Corporate Source: Universite Paul Sabatier, Toulouse, Fr
Conference Title: Proceedings of the 1995 22nd Annual International Symposium on Computer Architecture
Conference Location: Santa Margherita Ligure, Italy Conference Date: 19950622-19950624
Sponsor: ACM SIGARCH; IEEE
E.I. Conference No.: 43784
Source: Conference Proceedings - Annual International Symposium on Computer Architecture 1995.,95CH35801. p 117-125
Publication Year: 1995
CODEN: CPAADU ISSN: 0884-7495 ISBN: 0-7803-3000-5
Language: English
Document Type: CA; (Conference Article) Treatment: G; (General Review)
Journal Announcement: 9512W2
Abstract: This study has been carried out in order to determine cost-effective configurations of functional units for multiple-issue out-of-order superscalar processors. The trace-driven simulations were performed on the six integer and the fourteen floating-point programs from the SPEC 92 suite. We first evaluate the number of instructions allowed to be **concurrently** processed by the execution stages of the pipeline. We then apply some restrictions on the execution issue of different instruction classes in order to define these configurations. We conclude that five to nine functional units are necessary to exploit Instruction-Level Parallelism. An important point is that several data **cache** ports are required in a processor of degree 4 or more. Finally, we report on complementary results on the utilization rate of the functional units. (Author abstract) 15 Refs.
Descriptors: Computer architecture; Program processors; Microprocessor chips; **Parallel** processing systems; Data handling; Digital arithmetic; Computer simulation
Identifiers: Functional units; Out of order superscalar processor; Instruction level parallelism; Out of order execution
Classification Codes:
723.1 (Computer Programming); 722.1 (Data Storage, Equipment & Techniques); 722.4 (Digital Computers & Systems); 721.3 (Computer Circuits); 721.1 (Computer Theory, Includes Formal Logic, Automata Theory, Switching Theory, Programming Theory)
723 (Computer Software); 722 (Computer Hardware); 721 (Computer Circuits & Logic Elements)
72 (COMPUTERS & DATA PROCESSING)

32/5/2 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6346051 INSPEC Abstract Number: B1999-10-1265F-028, C1999-10-5130-014
Title: Correlated load-address predictors
Author(s): Bekerman, M.; **Jourdan, S.** ; Ronen, R.; Kirshenboim, G.; Rappoport, L.; Yoaz, A.; Weiser, U.
Author Affiliation: Intel Corp., Haifa, Israel
Conference Title: Proceedings of the 26th International Symposium on Computer Architecture (Cat. No.99CB36367) p.54-63
Publisher: IEEE Comput. Soc. Press, Los Alamitos, CA, USA
Publication Date: 1999 Country of Publication: USA xii+317 pp.
ISBN: 0 7695 0170 2 Material Identity Number: XX-1999-01337
U.S. Copyright Clearance Center Code: 1063-6897/99/$10.00
Conference Title: Proceedings of the International Symposium on Computer Architecture
Conference Sponsor: IEEE Comput. Soc. Tech. Committee on Comput. Archit.;

ACM SIGARCH
Conference Date: 2-4 May 1999 Conference Location: Atlanta, GA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Applications (A); Practical (P)
Abstract: As microprocessors become faster, the relative performance cost of memory accesses increases. Bigger and faster **caches** significantly reduce the absolute load-to-use time delay. However, increase in processor operational frequencies impairs the relative load-to-use latency, measured in processor cycles (e.g. from two cycles on the Pentium processor to three cycles of more in current designs). Load-address prediction techniques were introduced to partially cut the load-to-use latency. This paper focuses on advanced address-prediction schemes to further shorten program execution time. Existing address prediction schemes are capable of predicting simple address patterns, consisting mainly of constant addresses or stride-based addresses. This paper explores the characteristics of the remaining loads and suggests new enhanced techniques to improve prediction effectiveness: Context-based prediction to tackle part of the remaining, difficult-to-predict, load instructions. New prediction algorithms to take advantage of global correlation among different static loads. New confidence mechanisms to increase the correct prediction rate and to eliminate costly mispredictions. Mechanisms to prevent long or random address sequences from polluting the predictor data structures while providing some hysteresis behavior to the predictions. Such an enhanced address predictor accurately predicts 67% of all loads, while keeping the misprediction rate close to 1% We further prove that the proposed predictor works reasonably well in a deep pipelined architecture where the predict-to-update delay may significantly impair both prediction rate and accuracy. (12 Refs)
Subfile: B C
Descriptors: data structures; microprocessor chips; **parallel** architectures; performance evaluation
Identifiers: correlated load-address predictors; microprocessors; performance cost; load-to-use time delay; processor operational frequencies ; processor cycles; address-prediction schemes; program execution time; pipelined architecture
Class Codes: B1265F (Microprocessors and microcomputers); C5130 (Microprocessor chips); C6120 (File organisation); C5470 (Performance evaluation and testing); C5220P (Parallel architecture)

32/5/3 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

4916845 INSPEC Abstract Number: B9505-1265F-044, C9505-5130-007
Title: A high out-of-order issue symmetric superpipeline superscalar microprocessor
Author(s): **Jourdan, S.** ; Carriere, D.; Litaize, D.
Author Affiliation: Inst. de Recherche en Inf., Univ. Paul Sabatier, Toulouse, France
p.338-45
Publisher: IEEE Comput. Soc. Press, Los Alamitos, CA, USA
Publication Date: 1994 Country of Publication: USA xxi+720 pp.
ISBN: 0 8186 6430 4
U.S. Copyright Clearance Center Code: 0 8186 6430 4/94/$4.00
Conference Title: Proceedings of Twentieth Euromicro Conference. System Architecture and Integration
Conference Date: 5-8 Sept. 1994 Conference Location: Liverpool, UK
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: Due to technology's evolution, the number of transistors that can be integrated in a same chip has become, at the dawn of the 21st century, more than sufficient to implement simple superscalar cores. This excess, nowadays generally used for on-chip **caches** , can also be utilized to improve core's performances, but mainly to increase the core's superscalarness degree. Although it now seems that a high degree is not justified, it could become useful in the future with progress in

compilation. Setting out from this observation, we describe a new superscalar architecture with a high out-of-order issue rate. This architecture implements, in particular, precise interrupt management and multiple branch prediction. Furthermore, the architecture's specification has taken into account the aspect of hardware implementation, and thus, temporal matching of pipeline's stages. We therefore assist to a finer partitioning of this pipeline, hence the additional superpipeline label. (18 Refs)
Subfile: B C
Descriptors: microprocessor chips; **parallel** architectures
Identifiers: symmetric superpipeline superscalar microprocessor; on-chip **caches** ; interrupt management; multiple branch prediction; temporal matching
Class Codes: B1265F (Microprocessors and microcomputers); C5130 (Microprocessor chips); C5220P (Parallel architecture)

32/5/4 (Item 1 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

01054509 E96120414353
Multiple-block ahead branch predictors
(Ein Verzweigungspraediktor, der mehrfache Befehlsbloecke voraussieht)
Seznec, A; **Jourdan, S** ; Sainrat, P; Michaud, P
Campus de Beaulieu, Rennes, F; Univ. Paul Sabatier, Toulouse, F
Computer Architecture News, v24, nSpecial issue: ASPLOS-VII Proceedings, pp116-127, 1996
Document type: journal article Language: English
Record type: Abstract
ISSN: 0163-5964

ABSTRACT:
A basic rule in computer architecture is that a processor cannot execute an application faster than it fetches its instructions. This paper presents a novel cost-effective mechanism called the two-block ahead branch predictor. Information from the current instruction block is not used for predicting the address of the next instruction block, but rather for predicting the block following the next instruction block. This approach overcomes the instruction fetch bottle-neck exhibited by wide-dispatch 'brainiac' processors by enabling them to efficiently predict addresses of two instruction blocks in a single cycle. Furthermore, pipelining the branch prediction process can also be done by means of the authors predictor for 'speed demon' processors to achieve higher clock rate or to improve the prediction accuracy by means of bigger prediction structures. Moreover, and unlike the previously-proposed multiple predictor schemes, multiple-block ahead branch predictors can use any of the branch prediction schemes to perform the very accurate predictions required to achieve high-performance on superscalar processors.

DESCRIPTORS: **PARALLEL** PROCESSING; COMPUTER ARCHITECTURE; PROGRAM INSTRUCTION; COMMAND EXECUTION; COMMAND STRUCTURE; **CACHE** MEMORIES; FORECAST; THEORETICAL MODELS; MODEL STUDY; PERFORMANCE ANALYSIS; PERFORMANCE EVALUATION; **PARALLEL** PROGRAMMING; BUFFER STORAGE; PIPELINE PROCESSING; BENCHMARKING; ACCESS TIME; DATA STORAGE; REDUCED INSTRUCTION SET COMPUTER; JUMP INSTRUCTION
IDENTIFIERS: IF ABFRAGE; VERZWEIGUNGSVORHERSAGE; Verzweigungsvorhersage; Befehlsspeicherung; Architektur